


(※本報告書は英語で記述してください。ただし、産業利用課題として採択されている方は日本語で記述していただいても結構です。)

 MLF Experimental Report	提出日 Date of Report July 27, 2017
課題番号 Project No. 2016B0046 実験課題名 Title of experiment Measurement of single event upset rates for static random access memories induced by low energy positive and negative muons 実験責任者名 Name of principal investigator Yukinobu Watanabe 所属 Affiliation Kyushu University	装置責任者 Name of responsible person Yasuhiro Miyake 装置名 Name of Instrument/(BL No.) MUSE D2 instrument 実施日 Date of Experiment Feb. 28 – March 2, 2017

試料、実験方法、利用の結果得られた主なデータ、考察、結論等を、記述して下さい。(適宜、図表添付のこと)
 Please report your samples, experimental method and results, discussion and conclusions. Please add figures and tables for better explanation.

1. 試料 Name of sample(s) and chemical formula, or compositions including physical form.
Two kind of Static random access memories (SRAMs) 1) 65-nm bulk CMOS SRAM 2) 65-nm ultra-thin body and thin buried oxide (UTBB-SOI) SRAMs (Hereafter this is called SOTB)

2. 実験方法及び結果 (実験がうまくいかなかった場合、その理由を記述してください。) Experimental method and results. If you failed to conduct experiment as planned, please describe reasons.
<p>The accelerated test with both negative and positive muons was performed using the D2 experimental area at J-PARC Muon Facility, MUSE.</p> <p>The configuration of muon irradiation is schematically illustrated in Fig. 1. The beam collimator was placed between the beam exit and the device board. The size of the collimator slit was 50 mm × 50 mm. The collimator consisted of a 5-mm thick aluminum plate and piled-up 150-mm thick lead blocks. The lead blocks play a role in the shielding of decay electrons/positrons from the aluminum plate and background γ-rays. The device board was placed perpendicularly to the muon beam track. Twelve chips in the device were irradiated and the remaining four chips were placed behind the lead blocks in order to see the influence of background radiations in the environment.</p> <div data-bbox="925 1545 1420 1904" data-label="Diagram"> <p>The diagram shows a top-down view of the experimental setup. At the top, a muon beam (μ^{\pm}) is directed downwards through a 'Beam Exit' and a 'Beam Slit'. The collimator is positioned below the slit, consisting of a 5 mm thick 'Al Plate' and '150 mm thick' 'Pb Block' layers. The total height of the collimator assembly is 155 mm. Below the collimator is the 'Device Board', which is 35 mm thick. On the device board, there are 12 irradiated chips and 4 chips located behind the lead blocks.</p> </div> <p style="text-align: center;">Fig.1 Experimental layout</p>

2. 実験方法及び結果(つづき) Experimental method and results (continued)

The reverse side of the device board was irradiated with the muon beam passing through the collimator. Muons stopped in the device board undergo decay into electrons/positrons. They were measured by coincidence counting with two plastic scintillators placed at the downstream of the device board. Also, a germanium detector was placed to monitor the muonic X-rays under the negative muon irradiation. The data of the muonic X-rays can provide additional information on the position where negative muons stopped in the device board.

The irradiation tests with negative and positive muons were performed in the momentum range from 34 MeV/c to 44 MeV/c. The SEU cross section can be derived by dividing the number of the observed bit errors by the incident muon fluence. The fluence per proton beam pulse was determined by the total coincidence count of decay electrons/positrons from a pure aluminum plate placed instead of the device board, in advance of the irradiation tests.

As one of the preliminary experimental results, the measured SEU cross sections for SOTB SRAM with supply voltage of 0.5 V are plotted as a function of momentum in Fig. 2. Both the negative and positive muon SEU cross sections have the peaks around 38 MeV/c. Our preliminary simulation with the PHITS code shows that the 38-MeV/c muon can stop near the sensitive volume. This suggests that the muon deposits the maximum charge in the region localized at the end of its path and the deposited charge leads to higher probability of SEU occurrence. Next, it is found that the negative muon SEU cross sections are approximately three to four times higher than the positive muon SEU ones in the momentum range from 35 MeV/c to 39 MeV/c. From this result, the secondary ions generated from negative muon capture reaction are expected to cause SEUs more significantly than the direct ionization of muons. As the muon momentum is higher than 40 MeV/c, the difference between both muons in the SEU cross section is smaller and smaller, and both are almost the same over 42 MeV/c. Most of the muons with momentum over 42 MeV/c pass through the device board, and negative muon capture reaction seldom happens near the sensitive volume. Only the direct ionization contributes to the occurrence of SEUs. Thus, the difference between the positive and negative muon SEU cross sections is approximately equivalent to the contribution from secondary heavy and light ions generated by negative muon capture reactions in the device.

Detailed data analysis for both SOTB and Bulk SRAMs is now in progress.

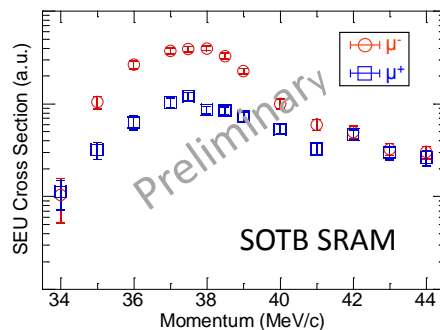


Fig.2 Measured cross sections of SEUs induced by negative and positive muons